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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,924	10/10/2001	Albrecht Mayer	J&R-0748	1097

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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,924	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/1/06 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8, 9 and 16 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 8 and 16 recites the limitation "units" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 10, 11 and 17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Swoboda et al. (US Patent 6,349,392).

7. As per claim 1:

A programmable unit, comprising:

at least one program running unit for running a program (Abstract);

a stopping device connected to said program operation unit, said stopping device issuing a stop command to said program operation unit to stop the running of the program by said program operation unit (Abstract);

other components connected to said stopping device, stop command causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated (Abstract); and

said other components including at least one further program operation unit or at least one peripheral which is not a further program operation unit, said stop command being selectively provided from said stopping device to said other component if said other component is said at least one further program operation unit and said stop command being directly provided from said stopping device to said other component if said other component is said at least one peripheral (Abstract).

8. As per claim 10:

The programmable unit according to claim 1, wherein said stopping device is an on-chip debug support module (column 2, lines 3-5).

9. Claims 11 and 17 recite similar limitations as claims 1 and 10 and are rejected for the same reasons.

Maintained Claim Rejections – 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison, EP 0 455 946 A2.

12. Regarding claim 1, Harrison, has taught a programmable unit, comprising:

a. At least one program operation unit for running a program [Processor 16 (PO 16), fig. 1 and col. 3, lines 11-19]

b. A stopping device (bus monitor 12, figures 1 and 2) connected to said program operation unit said stopping device stopping the running of the program by said program operation unit [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

c. Other components [P1-P7, fig. 1] connected to said stopping device said stopping device also issuing a stop command causing said other components to be stopped, in addition to stopping said program operation unit with which said

stopping device is associated: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

d. And said other components including at least one further program operation unit or at least one peripheral [P1-P7, fig. 1], said stopping command being selectively provided from said stopping device to said other component if said other component is said further program operation unit [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

e. And said stop command being directly provided from said stopping device to said other component if said other component is a peripheral: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

f. Examiner notes that the claim language only requires the other components to be *either* a further program operation unit *or* a peripheral, *not both.* However, The American Heritage Dictionary of the English Language, 4th Ed defines peripheral as, "An auxiliary device, such as a printer, modem, or storage system, that works in conjunction with a computer." It then defines auxiliary as, 1. Giving assistance or support; helping." A processor within a multiprocessor system is a peripheral to the other processors, and the other processors are peripherals to the processor, since each works in conjunction with a computer giving assistance or support to carry out data processing. Therefore, any of the processors, P1-P7 could be considered either a peripheral or a program operation unit.

However, Harrison has not taught wherein said stopping device is located on the same chip as said program operation unit.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the bus monitor 12 and the PO 16 onto a single chip since it has been held "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice." [In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)]

13. Regarding claim 2, Harrison has taught the programmable unit according to claim 1, wherein said other components [P1-P7, fig.1] include at least one further program operation unit and said stopping device able to stop said further program operation unit which is not associated with said stopping device. [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

14. Regarding claim 3, Harrison has taught the programmable unit of claim 2, wherein said other components [P1-P7, fig. 1] which can be stopped by said stopping device include units which are connected to and cooperate with said program operation unit and said further program operation unit: [Col. 3, line 42 to col. 4, line 24, col. 8, line 55 to col. 9, line 16 and figure 4.]

15. Regarding claim 4, Harrison has taught the programmable unit of claim 3, wherein said units are stopped by said stopping device later in time than said program operation unit and said further program operation unit: [The processors (P1-P7) can be selectively stopped, depending on the settings within bus monitor 12. The settings are alterable, i.e., the bus monitor can be set up to issue stop commands to certain

processors at one point during processing, then the set-up can be altered so that different processors are issued the stop command. [Fig. 5, and col. 9, lines 17-35] Therefore, some units (e.g., PO 3 and 4) can be initially not given the stop command upon a first breakpoint. Then, the bus monitor 12 can be reconfigured so that upon another breakpoint (later in time), the units (PO 3 and 4) will be issued a stop command.]

16. Regarding claim 5, Harrison has taught the programmable unit of claim 4, including at least one bus connected between said other components [Figure 1]

17. Regarding claim 6, Harrison has taught the programmable unit of claim 5, including bus interfaces and each of said bus interfaces is connected to one of said program operation unit and said further program running unit and to said bus: The program operation unit [P0] and further program running unit [Any of [P1-P7]: Each of the processors [P0-P7] is connected to a bus as shown in figure 1, [Shared-Memory Bus 15]. Interface is defined as, "A surface forming a common boundary between adjacent regions, bodies, substances, or phases. 2. A point at which independent systems or diverse groups interact. 3. *Computer Science* a. The point of interaction or communication between a computer and any other entity, such as a printer or human operator." (The American Heritage College Dictionary, 4th Edition) Therefore, since the bus is connected to both the program operation unit and said further program running unit, there is an interface present at the connection point, in which both the bus and the program operation unit or said further program unit are connected.

-Said program operation unit and said further program operation unit function as bus masters: [Each of the processors (P0-P7) operate as bus masters since each has memory controller. When a processor has access to the shared bus to communicate with the shared memory (Read or Write), it is functioning as a bus master. Col. 3, lines 20-34, figure 1.]

Harrison teaches where the bus monitor 12 selectively issues the stop command (an interrupt) to processors (P0-P7) and wherein the interrupts is assigned a priority level by the bus monitor 12 as well. However, the priority level of the stop command is not specifically assigned, it is only stated that "the bus monitor 12 is configured to identify which processors are to be interrupts and an interrupt level to be used." (Col. 4, lines 12-14). Therefore, Harrison does not explicitly teach where said units are stopped only when said bus masters and said bus interfaces have no more data to output and/or are no longer waiting for already requested data or data that is still to be requested.

One of ordinary skill in the art would have recognized to set the interrupt level in such a way as to allow the current pending transactions to be completed by the processor so as to allow the pending instructions to be completed before probing of the processors is begun. This will allow a known architected state to be debugged, as opposed to a possibly unknown state, which is what may occur when an interrupt is given a higher priority than the pending bus/memory operations. Therefore, it would have been obvious to one of ordinary skill in the art to have a low-enough interrupt level associated with the stop command (breakpoint interrupts) so as to allow the bus

masters and bus interfaces to wait for pending operations to be completed before the interrupt occurs.

18. Regarding claim 7, Harrison has taught the programmable unit according to claim 5, wherein said bus includes a first bus part, a second bus part and a bus bridge connecting said first bus part to said second bus part: [Figure 1. Each vertical line portion of Shared – Memory Bus 15 is a "bus part". The horizontal line portion of Shared – Memory Bus 15 is the "bus bridge" connecting said first bus part to said second bus part.]

Harrison teaches where the bus monitor 12 selectively issues the stop command (an interrupt) to processors (P0-P7) and wherein the interrupts is assigned a priority level by the bus monitor 12 as well. However, the priority level of the stop command is not specifically assigned, it is only stated that "the bus monitor 12 is configured to identify which processors are to be interrupts and an interrupt level to be used." (Col. 4, lines 12-14). Therefore, Harrison does not explicitly teach wherein said units are stopped only when said bus bridge has no more data to pass on.

One of ordinary skill in the art would have recognized to set the interrupt level in such a way as to allow the current pending transactions to be completed by the processor so as to allow the pending instructions to be completed before probing of the processors is begun. This will allow a known architected state to be debugged, as opposed to a possibly unknown state, which is what may occur when an interrupt is given a higher priority than the pending bus/memory operations. Therefore, it would have been obvious to one of ordinary skill in the art to have a low-enough interrupt level

associated with the stop command (breakpoint interrupts) so as to allow the bus masters and bus interfaces to wait for pending operations to be completed before the interrupt occurs.

19. Regarding claim 10, Harrison has taught the programmable unit of claim 1, wherein said stopping device is an on-chip debug support module. [It is inherent that the stopping device (bus monitor 12) is designed/made on a chip because it contains hardware and logic as shown in figure 2. Harrison discloses there the bus monitor device is used for debugging and monitoring. [Col. 3, line 42 to col. 4, line 39]

20. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison, EP 0 455 946 A2, and further in view of Wen et al., U.S. Patent 5,956,514, herein referred to as Wen.

21. Regarding claim 8, Harrison has taught the programmable unit of claim 1, but does not give a thorough disclosure of the restarting of the application on the parallel processors (P0-P7). Harrison only states that the Processor 16 (P0) runs the debugging program and it issues a command to resume execution of the application when the debugging is completed. Therefore, processor 16 (P0) is the master processor, and the others are slaves.

However, Harrison fails to teach wherein after a stopped state of components of the programmable unit which have been stopped is cancelled, said units recommence operation before said program operation unit and said further program operation unit recommence operation.

Wen teaches wherein after a breakpoint, and debugging, the Master processor can issue a restart command [unhold_cpu()] to individual slave processors. The restart command can either indicate to start the application over from the beginning or to resume at the point from which it was interrupted at. This allows a greater degree of flexibility for the programmer, because it is possible to selectively restart processors. [Col. 6, lines 41-64 and figure 1] This is similar to Harrison's teaching for selectively issuing the stop commands, which has the of increased flexibility for debugging purposes. Adding this feature to Harrison would cause the P0 processor to cause the "units" to recommence processing before the P0 processors does, and also at different times from each other. Therefore, the restarting command would cause the "units" to recommence operation before said program operation unit and said further program operation unit.

It would have been obvious to one of ordinary skill in the art to use the teachings of Wen, wherein slave processors can be selectively resumed, since it would increase the flexibility of the debugging process.

22. Regarding claim 9, given the similarities between claim 8 and claim 9, the arguments as stated for claim 8 are also applicable to claim 9.

23. Claims 11-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison in further view of Swoboda.

24. As per claim 11:

Harrison teaches claim 1 for the reasons stated above.

The only difference between claim 1 and 11 is that "other components" are exclusively peripherals that are not program operation units in claim 11.

Harrison does not teach extending his stopping system to other peripherals.

However, Swoboda does (Swoboda: Abstract).

Swoboda states that *all* ICs in a circuit should be thoroughly tested in end systems to ensure that the ICs work in systems where life literally depends on their compliance (Swoboda: column 2, lines 24-32).

Harrison would be motivated to test peripherals as in Swoboda for safety issues and to prevent the loss of human life.

25. Claims 12-15 and 17 recite similar limitations as claims 4-7 and 10, respectively, and are rejected for the same reasons listed above.

26. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrison in combination with Swoboda as applied claim 11 above and in further view of Wen.

27. The combination of Harrison and Swoboda fail to teach wherein after a stopped state of components of the programmable unit which have been stopped is cancelled, said units recommence operation before said program operation unit and said further program operation unit recommence operation.

Wen teaches wherein after a breakpoint, and debugging, the Master processor can issue a restart command [unhold_cpu()] to individual slave processors. The restart command can either indicate to start the application over from the beginning or to resume at the point from which it was interrupted at. This allows a greater degree of flexibility for the programmer, because it is possible to selectively restart processors.

[Col. 6, lines 41-64 and figure 1] This is similar to Harrison's teaching for selectively issuing the stop commands, which has the of increased flexibility for debugging purposes. Adding this feature to Harrison would cause the P0 processor to cause the "units" to recommence processing before the P0 processors does, and also at different times from each other. Therefore, the restarting command would cause the "units" to recommence operation before said program operation unit and said further program operation unit.

It would have been obvious to one of ordinary skill in the art to use the teachings of Wen, wherein slave processors can be selectively resumed, since it would increase the flexibility of the debugging process.

Response to Arguments

28. The applicant argues that Harrison no longer anticipates the claims because Harrison does not teach stopping a peripheral device that is not a program operation unit in addition to the program operation unit.

While Harrison may not teach stopping a peripheral device that is not a program operation unit in addition to the program operation unit, the applicant's argument is moot with respect to claim 1 because the current claim limitation recites that the "other components" may be "at least one further program operation unit ***or*** at least one peripheral which is not a further program operation unit," (emphasis added). The claim

limitation is written in the alternative which means that Harrison still reads on the claim as presently amended.

However, the examiner agrees that the amendment to claim 11 overcomes Harrison.

29. The applicant has made the following argument:

> "HARRISON neither teaches, nor suggests, that once an interrupt is produced to processor P0 of Fig. 1 of HARRISON, that the interrupt may also be selectively provided to at least one of the processors P1-P7 of HARRISON, as required by Applicant's claim 1 when the "other components" include at least one further program operation unit."

The examiner asserts that when the interrupt is selectively produced, it will also be selectively provided; it would be pointless to provide an interrupt that doesn't exist.

Conclusion

Please note that the junior examiner of record has changed. Any further inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183

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